REMARKS/ARGUMENTS

This Amendment is in response to the Office Action dated April 6, 2004. Claims 1-10 are pending in the present application. Claims 1-10 have been rejected. Claims 1, 6, 8, and 9 have been amended to further define the scope and novelty of the present invention. Support for the amendments to the claims are found throughout the specification, and in particular, in Figure 2A and the accompanying text. Applicants respectfully submit that no new matter has been presented. Claim 10 has been canceled. Accordingly, claims 1-9 remain pending. For the reasons set forth more fully below, Applicants respectfully submit that the claims as presented are allowable. Consequently, reconsideration, allowance, and passage to issue are respectfully requested.

Claim Rejections - 35 U.S.C. §112

The Examiner has stated:

> **Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.**
>
> **The recitation that the size of the second latch is "minimized" compared to the size of the first latch is vague and indefinite. It cannot be determined if this simply means that the second latch is smaller than the first latch, or whether it means that the second latch is made as small as possible (the standard definition given in a dictionary). Because the specification does not clearly define this term, and because it is not clear how this feature of the invention distinguished over the applied prior art, see paragraph four below, this terminology does not pass muster under U.S.C. 112, second paragraph.**

In response, claims 1, 6, 8, and 9 have been amended to address the above-referenced rejections. Specifically, these claims have been amended such that "the size of the second latch is smaller than the size of the first latch." Applicants respectfully submit that the claims as amended now comply with 35 U.S.C. 112, second paragraph.

Claim Rejections - 35 U.S.C. §102

The Examiner has stated:

> **Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Gregor et al.**
>
> **See paragraph three of the previous office action mailed on 8/21/03 for the details of this rejection. The new limitation is vague and indefinite, as noted above, and therefore cannot be relied upon to define over Gregor et al...**
>
> **The argument that Gregor et al. does not disclose first and second clocks is not persuasive because, as noted in the rejection, the claimed first clock reads on signal C1 and the claimed second clock reads on either signal C2 or the signal at terminal C of slave latch 22.**
>
> **The argument that the second latch in Gregor et al cannot be minimized because it performs a performance critical function is not persuasive because it is not understood why it is performance critical in the reference but not performance critical in the instant invention. Since the claimed structure is fully anticipated by Gregor et al, any size minimization that can be achieved in applicant's circuitry can of course be achieved in the circuitry of Grgeor et al.**

Applicants respectfully traverse the Examiner's rejections. For the Examiner's convenience, amended independent claim 1 is reproduced in its entirety herein below.

Claim 1

> 1. (currently amended) A flip-flop comprising:
> a first latch for receiving at least one bit;
> a second latch coupled to the first latch for storing the at least one bit from the first latch, wherein the size of the second latch is smaller than the size of the first latch to reduce power consumption; and
> a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active.

The present invention as recited in varying scope in amended independent claims 1, 6, 8, and 9 is directed toward a system and method for optimizing power consumption in a flip-flop. The flip-flop comprises a first latch for receiving at least one bit and a second latch coupled to the first latch for storing the at least one bit from the first latch. The size of the second latch is smaller than the size of the first latch to reduce power consumption. The flip-flop also comprises

a multiplexor for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active (Summary and Fig. 2B and the accompanying text).

In accordance with present invention, the first clock is used to pass data at a significantly fast rate by outputting data directly from the first latch to the multiplexor. In addition, the second clock is used to store data in the second latch and later output the data to the multiplexor. Typically, in a slave configuration, the most performance-critical function is the launch time of slave latch (i.e., the second latch). Here, however, the first latch performs the most performance-critical function because it passes data directly to the multiplexor. The second latch no longer serves a performance-critical function because it is used to store data. Because the second latch does not serve a performance-critical function, it can be implemented using minimum sized devices to reduce power consumption (Specification generally, Summary).

Gregor discloses a scannable double-edge-triggered flip-flop having two latches and a multiplexor, all of which are driven by a single clock. Each latch has a plurality of inputs and is coupled to the clock, which provides a clock signal, via a means for providing a delayed version of the clock signal. The multiplexor has (i) inputs fed by outputs of the latches, and (ii) a select input fed by the clock signal, and means for providing a select signal for selecting the latch whose clock is inactive. Each latch has a scan input gate and a scan output gate, and the scan output of the first latch is applied to the scan input of the second latch to form a scannable latch pair (Abstract and Fig. 2).

However, Gregor does not teach or suggest the first and second latches, "wherein the size of the second latch is smaller than the size of the first latch to reduce power consumption," as

recited in amended independent claim 1. Instead, Gregor teaches reducing a clock speed to reduce power consumption (column 1, lines 31-45). Nowhere does Gregor specifically teach making the size of a second latch smaller than the size of a first latch to reduce power consumption as in the present invention. The Examiner has stated that it is not understood why the second latch is performance critical in the reference, but not performance critical in the instant invention. In Gregor, both latches are performance critical because they are used in a double-edge triggered flip-flop, which is designed for high performance. Double-edge triggered flip-flops are fast because one latch clocks at clock=0 and the other latch clocks at clock=1 (column 3, lines 11-16). This increases the performance suggesting that both latches are performance critical.

Furthermore, referring to Figures 2 and 8-11 of Gregor and the corresponding descriptions, the two latches appear to be identical. Referring to the timing diagram of Figure 5, the output speed of the data output at every edge is identical. This strongly suggests that both latches of Gregor are the same size.

In contrast to the latches of Gregor, the first and second latches of the present invention are not used in a double-edge triggered flip-flop but are instead used in a master-slave flip-flop. Typically, in a slave configuration, the most performance-critical function is the launch time of slave latch (i.e., the second latch). However, in the present invention, the first latch performs the most performance-critical function because it passes data directly to the multiplexor. The second latch does not serve a performance-critical function because it is used to store data. Because the second latch does not serve a performance-critical function, it can be implemented using minimum sized devices to reduce power consumption (Specification generally, Summary).

Referring to Figure 2B of the present invention, the switching speed "y" of the slave latch is slower than the switching speed "x" of the master latch. This is different from Gregor where the latches operate at the same speed (Figure 5).

Therefore, Gregor does not teach or suggest the cooperation of elements as recited in the present invention. Accordingly, claim 1 is allowable over Gregor.

Independent claims 6, 8, and 9

Similar to amended independent claim 1, amended independent claims 6, 8, and 9 recite a first/master latch and a second/slave latch, wherein the size of the second/slave latch is "smaller than the size of" the first/master latch to reduce power consumption. As described above, with respect to amended independent claim 1, Gregor does not teach or suggest this feature. Accordingly, the above-articulated arguments related to amended independent claim 1 applies with equal force to claims 6, 8, and 9. Therefore, these claims are allowable over Gregor for at least the same reasons as claim 1.

Remaining dependent claims

Dependent claims 2-5 and 7 depend from amended independent claims 1 and 6, respectively. Accordingly, the above-articulated arguments related to amended independent claims 1 and 6 apply with equal force to claims 2-5 and 7, which are thus allowable over the cited reference for at least the same reasons as claims 1 and 6.

Conclusion

In view of the foregoing, Applicants submit that claims 1-9 are patentable over the cited reference. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

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Date

Stephen G. Sullivan
Attorney for Applicant(s)
Reg. No. 38,329
(650) 493-4540